18. (New) A method as defined in claim 17, wherein the diode is implemented by fabricating a P-type region in an N-type region, and fabricating the N-type region in the cathode-gate region of the anode-gate thyristor on the front surface of the substrate.

19. (New) A method as defined in claim 15, further comprising fabricating a second gate current amplification transistor in the substrate, wherein the second transistor is associated with the anode-gate thyristor.

20. (New) A method as defined in claim 19, wherein the second transistor is fabricated on the front surface of the substrate with a collector region of the second transistor extending via isolating walls toward the lower surface of the substrate and being in contact with the lower surface metallization.

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21. (New) A method as defined in claim 15, further comprising connecting the cathode-gate thyristor and the anode-gate thyristor in antiparallel between a first terminal of the line to be protected and a reference voltage, connecting the gate of the cathode-gate thyristor to a negative threshold voltage via the first gate current amplification transistor, and connecting the gate of the anode-gate thyristor to a positive threshold voltage.

22. (New) A method as defined in claim 21, further comprising connecting the gate of the cathode-gate thyristor to a second terminal of the line to be protected.

23. (New) A method as defined in claim 21, further comprising connecting the gates of the cathode-gate and anode-gate thyristors to a second terminal of the line to be protected.

REMARKS

By this preliminary amendment, new claims 6-23 have been added and claims 1-5 have been amended. Accordingly, claims 1-23 are pending in the application. No new matter has been added.

In addition, the specification has been amended to correct obvious errors. In particular, most instances of "smaller" have been changed to "lower" to correct an apparent error in word selection. The reference characters T′1, Th′1 and Th′2 have been changed to T1′, Th1′ and Th2′, respectively, for consistency with the reference characters used in the drawings. No new matter has been added. Section headings have also been added.

The application is now ready for examination on the merits. If there are questions regarding this preliminary amendment, please contact Applicant's undersigned attorney.

Respectfully submitted,
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MARKED-UP SPECIFICATION

The paragraph beginning at page 1, line 1 has been amended as follows:

Background Of The Invention

1. Field of the Invention

The present invention relates to circuits that protect against overvoltages, which circuits can be used in particular for subscriber line interface circuits (SLIC).

The paragraph beginning at page 1, line 4 has been amended as follows:

2. Discussion of the Related Art

Telephone circuits connected to lines are particularly likely to be disturbed by overvoltages such as lightning discharges or accidental connections to lines of the electric power network. Further, the problem of the protection of interface circuits becomes more and more acute as these interface circuits are formed of more and more integrated circuits of smaller and smaller dimensions and accordingly, more and more sensitive to overvoltages.

The paragraph beginning at page 1, line 16 has been amended as follows:

Summary Of The Invention

The present invention aims at implementing a monolithic protection circuit capable of establishing a short-circuit between each conductor of a line and a ground when the voltage on this conductor exceeds a determined positive threshold or becomes [smaller] lower than a predetermined negative threshold.

The paragraph beginning at page 2, line 13 has been amended as follows:

To achieve these objects, the present invention provides a monolithic component that protects against line overvoltages greater than a determined positive threshold or [smaller] lower than a determined negative threshold, including in antiparallel a cathode-gate thyristor and an anode-gate thyristor connected between a first terminal of the line to be protected and a reference voltage, the gate of the cathode-gate thyristor being connected to a negative threshold voltage via a gate current amplification transistor, the gate of the anode-gate thyristor being connected to a positive threshold voltage. The monolithic component is made in a substrate of the first

conductivity type divided into wells separated by isolating walls, the [smaller] lower surfaces of which are coated with insulating layers, the [smaller] lower surface of the substrate being uniformly coated with a metallization. The gate current amplification transistor of the cathode-gate thyristor is made in vertical form in a first well. The cathode-gate thyristor is implemented in vertical form in a second well. The anode-gate thyristor is implemented in vertical form in a third well. The [smaller] lower surface metallization links up the collector of the transistor, the anode of the cathode-gate thyristor, and the cathode of the anode-gate thyristor. A first front surface metallization connects the cathode of the cathode-gate thyristor to the anode of the anode-gate thyristor. A second front surface metallization connects the gate of the cathode-gate thyristor to the emitter of the transistor. A third front surface metallization is in contact with the gate of the anode-gate thyristor.

The paragraph beginning at page 3, line 9 has been amended as follows:

According to an embodiment of the present invention, the gate of the cathode-gate thyristor is connected to a second terminal of the line to be protected associated with the anode-gate thyristor, this transistor, of PNP type, being formed on the upper surface of the component, the collector region extending via isolating walls towards the [smaller] lower surface and being in contact with the [smaller] lower surface metallization.

The paragraph beginning at page 3, line 16 has been amended as follows:

Brief Description Of The Drawings

The foregoing objects, features and advantages of the present invention, will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings wherein:

The paragraph beginning at page 3, line 33 has been amended as follows:

Detailed Description

Fig. 1A shows a circuit that protects against overvoltages and overcurrents on a telephone line L1-L2. Each of the conductors of the telephone line includes a series resistor, respectively R1, R2, enabling to detect overcurrents. The terminals of resistor R1 which form first input

terminals of the circuit according to the present invention will be called L1A and L1B and the terminals of resistor R2 which form second input terminals of the circuit will be called L2A and L2B. Between terminal L1A and a reference potential, currently the ground, two antiparallel thyristors, that is, a cathode-gate thyristor Th1 and an anode-gate thyristor Th2, are arranged. The anode of thyristor Th1 and the cathode of thyristor Th2 are grounded, and the cathode of thyristor Th1 and the anode of thyristor Th2 are connected to terminal L1A. The gate of the cathode-gate thyristor is connected to a negative voltage source –V via an NPN-type amplifier transistor T1. The gate of the anode-gate thyristor is connected to a positive voltage source +V (in this embodiment, via a diode D1). The gates of thyristors Th1 and Th2 are connected to terminal L1B. The emitter of transistor T1 is connected to terminal L1B, its collector to the ground and its base to negative voltage –V. This assembly forms the system of protection against overvoltages and overcurrents of conductor L1. Symmetrically arranged components designated by dashed references form the protection against overvoltages and overcurrents of line L2. The operation of this circuit which will be better understood by referring to the patents and patent applications of the applicant mentioned hereabove is the following.

The paragraph beginning at page 4, line 27 has been amended as follows:

- If a negative overvoltage [smaller] lower than voltage –V occurs on conductor L1, cathode-gate thyristor Th1 turns on and the negative overvoltage flows towards the ground. Transistor T1 increases the triggering sensitivity by acting as a gate amplifier.

The paragraph beginning at page 5, line 1 has been amended as follows:

A device that protects against overvoltages and overcurrents on conductor L1 has thus effectively been obtained. The [smaller] lower portion of the circuit performs the same function for conductor L2.

The paragraph beginning at page 5, line 17 has been amended as follows:

The component of Fig. 1B is formed from an N-type substrate 1 divided into three wells by isolating walls 3 and 4. Each isolating wall is formed by a P-type drive-in extending from the upper and [smaller] lower surfaces of the layer, with these diffusions joining substantially at the

middle of the wafer. The component is performed in a semiconductor power component technology in which a single metallization M1 covers the entire [smaller] lower surface or rear surface of the component. According to an aspect of the present invention, a technology in which the apparent portion of each isolating wall on the [smaller] lower surface side is insulated by an insulating layer is used. Reference 5 designates an insulating layer, currently silicon oxide, formed under the [smaller] lower surface of isolating wall 3 and reference 6 designates an insulating layer formed under the [smaller] lower surface of isolating wall 4.

The paragraph beginning at page 5, line 31 has been amended as follows:

Transistor T1 is formed in the left-hand well. This transistor is of vertical type and includes on the upper surface side a P-type base region 10 containing an N-type emitter region 11. On the [smaller] lower surface side is formed an N^+-type region 12 forming the collector contact recovered by metallization M1. It should be noted that insulating layer 5 extends so that metallization M1 contacts N region 12 and not substrate 1 of the well. An advantage of implementing this transistor in vertical form is that it can easily withstand relatively high voltages (voltage –V is for example -50 V). Further, the connection between the collector of this transistor and the anode of cathode-gate thyristor Th1 is performed in a particularly simple and efficient way by the rear surface metallization. Further, transistor T1 has a high gain (on the order of 80 to 200) which results in a particularly low current to be supplied by battery –V upon each triggering.

The paragraph beginning at page 6, line 11 has been amended as follows:

Cathode-gate thyristor Th1 is formed in the central well of Fig. 1B. It is implemented in vertical form. It includes on the [smaller] lower surface side an anode region 30 and on the upper surface side a P-type region 31 and an N-type cathode region 32, currently provided with emitter short-circuits. It should be noted that insulating regions 5 and 6 extend to P region 30 so that metallization M1 does not contact the N-type central well.

The paragraph beginning at page 6, line 18 has been amended as follows:

In the right-hand well of Fig. 1B are formed anode-gate thyristor Th2 and diode D1. Thyristor Th2 is made in the same way as thyristor Th1 in vertical form. It includes on the [smaller] lower surface side an N cathode region 40, and on the upper surface side a deep lightly-doped P-type region 42 (made at the same time as anode region 30 of thyristor Th1) in which are formed an N-type region 43 and a P-type anode region 44. Conventionally, the anode region is provided with emitter short-circuits. Diode D1 is formed in P-type region 42 and includes in this region an N-type region 45 forming its cathode and a P-type region 46 forming its anode. This diode is a lateral diode.

The paragraph beginning at page 7, line 20 has been amended as follows:

Fig. 2A shows an alternative of the circuit of Fig. 1A. Elements T1, Th1, Th2, [T'1] T1', [Th'1] Th1', [Th'2] Th2' reappear therein. The difference with Fig. 1A is that the gate of anode-gate thyristor Th2 is not connected to the gate of cathode-gate thyristor Th1 and is directly connected, as well as the gate of anode-gate thyristor [Th'2] Th2' to positive reference voltage +V. This circuit is simpler but does not protect against positive overcurrents. It however has the advantage that the anode-gate thyristor is particularly sensitive due to the absence of anode short-circuits.

The paragraph beginning at page 8, line 8 has been amended as follows:

Fig. 3A shows another alternative of the circuit according to the present invention. This time, the structure is completely symmetrical, that is, anode-gate thyristor Th2 is, like cathode-gate thyristor Th1, associated with a gate current amplification transistor. This transistor is designated with reference T2 for thyristor Th2 and with reference T2' for thyristor Th2'. Transistors T2 and T2' are PNP transistors while transistors T1 and [T'1] T1' are NPN transistors.

The paragraph beginning at page 8, line 16 has been amended as follows:

An implementation according to the present invention in monolithic form of the circuit of Fig. 3A appears in a simplified cross-section in Fig. 3B. Transistor T1 and transistor Th1 are

implemented in the same way as in the embodiments of Figs. 1B and 2B. Thyristor Th2 is implemented in the same way as that of Fig. 1B or of Fig. 2B according to the sensitivity desired for this thyristor. Transistor T2 is implemented between the wells containing thyristors Th1 and Th2. The collector of this transistor is formed of a P-type layer 61 deeply diffused from the upper surface. Region 61 is surrounded with a P-type drive-in 62 which joins a P-type region 63 formed from the [smaller] lower surface and on which is recovered the collector contact by metallization M1. Inside collector region 61 are formed a base region 64 and a P-type emitter region 65.

The paragraph beginning at page 9, line 4 has been amended as follows:

Fig. 4A shows an alternative of the circuit of Fig. 1A. This simpler circuit does not protect against overcurrents. Elements T1, Th1, Th2, [T'1] T1', [Th'1] Th1', [Th'2] Th2' reappear therein. The difference with Fig. 1A is that the gates of anode-gate thyristor Th2 and cathode-gate thyristor Th1 are neither interconnected, nor connected to terminal L1B which does not exist, resistor R1 being absent.

MARKED-UP CLAIMS

Claims 1-5 have been amended as follows:

1. (Amended) A monolithic component protecting a line against overvoltages greater than a determined positive threshold or [smaller] lower than a determined negative threshold, including in antiparallel a cathode-gate thyristor [(Th1)] and an anode-gate thyristor [(Th2)] connected between a first terminal [(L1A)] of the line to be protected and a reference voltage, the gate of the cathode-gate thyristor being connected to a negative threshold voltage [(-V)] via a gate current amplification transistor [(T1)], the gate of the anode-gate thyristor being connected to a positive threshold voltage [(+V)], characterized in that:

- the monolithic component is made in a substrate of [the] a first conductivity type divided into wells separated by isolating walls [(3, 4)], [the smaller] lower surfaces of which are coated with insulating layers [(5, 6)], [the smaller] a lower surface of the substrate being uniformly coated with a lower surface metallization [(M1)],
- the gate current amplification transistor [(T1)] of the cathode-gate thyristor is made in vertical form in a first well,
- the cathode-gate thyristor [(Th1)] is implemented in vertical form in a [third] second well,
- the [smaller] lower surface metallization [(M1)] links up the collector of the transistor, the anode of the cathode-gate thyristor, and the cathode of the anode-gate thyristor,
- a first front surface metallization [(M2)] connects the cathode of the cathode-gate thyristor to the anode of the anode-gate thyristor,
- a second front surface metallization [(M3)] connects the gate of the cathode-gate thyristor to the emitter of the transistor, and
- a third front surface metallization is in contact with the gate of the anode-gate thyristor.

2. (Amended) The component of claim 1, further including a diode [(D1)], the anode of which is connected to the gate of the anode-gate thyristor, characterized in that the diode is implemented in the form of a P-type region [(46)] itself formed in an N-type region [(45)], the

latter being formed in the cathode-gate region [(42)] of the anode-gate thyristor, on the upper surface side of the component.

3. (Amended) The component of claim 1, wherein the gate of the cathode-gate thyristor is connected to a second terminal of the line to be protected [(L1B)].

4. (Amended) The component of claim 1 [or 2], further ensuring a protective function against overcurrents, in which the gates of the cathode-gate and anode-gate thyristors are interconnected and connected to a second terminal of the line to be protected [(L1B)].

5. (Amended) The component of claim 4 [taken as attached to claim 1], further including a gate current amplification transistor [(T2)] associated with the anode-gate thyristor, characterized in that this transistor, of PNP type, is formed on the upper surface of the component, [the] a collector region [(61)] extending via isolating walls [(62, 63)] towards the [smaller] lower surface and being in contact with the [smaller] lower surface metallization [(M1)].